SIOV metal oxide varistors

Application notes

Date: January 2018

EPCOS AG is a TDK Group Company.

1 Applications

1.1 Protective circuits

The varistors must on all accounts be connected parallel to the electronic circuits to be protected.

Circuit concept, power supply line-to-line protection

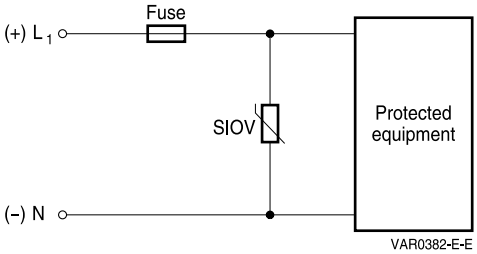


Figure 1 AC/DC single-phase protection

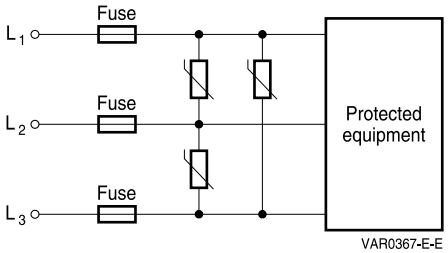


Figure 2 AC three-phase protection

When varistors are used in line-to-ground circuits (figures 3 and 4), the risk must be considered that a current type fuse may possibly not blow if the grounding resistance is too high and in this way the current is limited. With regard to such cases, various international and local standards do not allow the line-to-ground application of varistors without taking adequate safety countermeasures.

One possible solution is to use thermal fuses in series, which are thermally coupled with the varistor, as indicated in figures 3 and 4.

Circuit concept, power supply line-to-ground protection

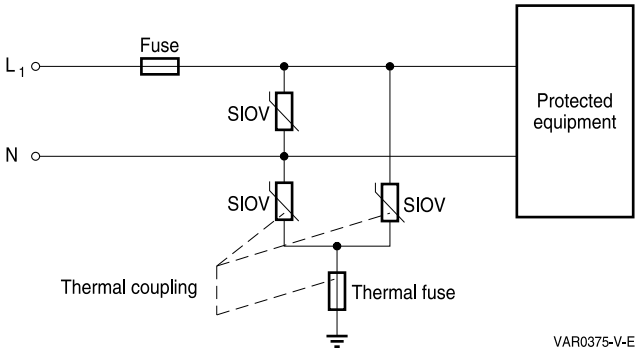


Figure 3 Single-phase protection including line-to-ground protection

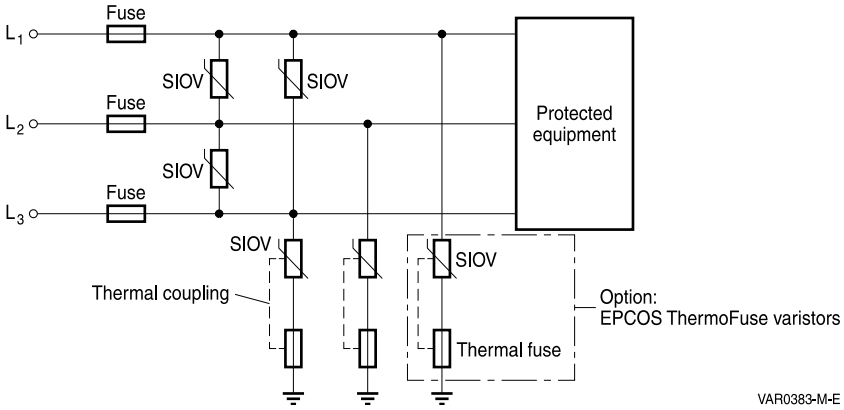


Figure 4 Three-phase protection including line-to-ground protection

Further typical applications of varistors used as a freewheeling circuit

Switching off protection

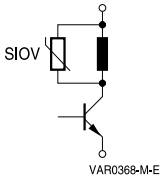


Figure 5

Semiconductor protection

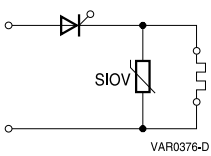


Figure 6

Contact spark suppression

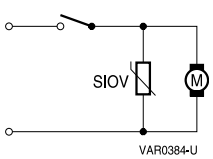


Figure 7

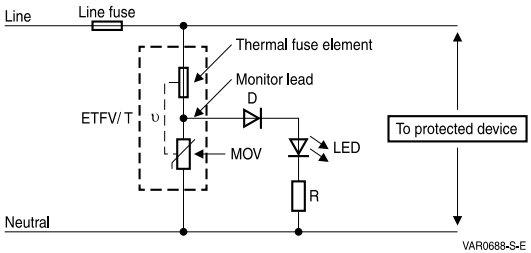


Figure 8 ETFV/ T single-phase protection with working condition indicator

1.2 Burst

According to IEC 61000-4-4, burst pulses are low-energy transients with steep edges and high repetition rate. Thus, for equipment to pass burst testing successfully, design (line filter, grounding concept, case) is as critical as the choice of varistor. If IEC 61000-4-5 has been taken into account when selecting varistors, they will normally also handle the burst pulse energy without any problems. Due to the steepness of the pulse edges, the varistors must be connected in a way that keeps parasitic circuit inductance low. The EPCOS EMC laboratory will carry out tests upon request (cf. 1.6).

1.3 Surge voltages

Immunity to interference from surge voltages (high energy) is tested in accordance with IEC 61000-4-5. The transient is generated using a combination wave (hybrid) generator.

The severity level to be applied in the immunity test must be defined as a function of installation conditions.

In most cases the respective product standards demand five positive and five negative voltage pulses. Standard IEC 61000-4-5 specifies severity level 3 (line-to-line, 2 kV applied via 2 Ω) as being the highest energy load. Table 2 illustrates that even the small varistor size SIOV-S10 is suitable for absorbing this energy level.

The table also shows assessments for the other severity level. The maximum current and voltage values given were calculated using PSpice.

Table 2 has been supplemented by the 4 kV test level. The application of this test level has

proven its worth in device protection for AC power supplies (without primary protection). Even this case can be dealt with using varistors of the standard series SIOV-S20, or, in case of space limitations, by using the decreased-size EnergetiQ series SIOV-Q14.

For the immunity testing line-to-earth of power supplies, IEC 61000-4-5 specifies 12 Ω as the internal resistance of the test generator. The energy content, which is considerably lowered due to this, permits use of the “small” type series SIOV-S05 and SIOV-S07.

For all other types of line, the internal resistance of the generator should be set to 42 Ω.

Note:
Connection of varistors to ground may be subject to restrictions. This must be clarified with the respective authorization offices.

Table 2

Application		2 Ω, 10 load cycles					
AC power supply line-to-line		230 V_{RMS}			400 V_{RMS}		
Severity level	kV	Type	I^*_{max} A	V^*_{max} V	Type	I^*_{max} A	V^*_{max} V
1	0.5	overvoltage protection not necessary					
2	1	S07K275	135	820	S05K460	3	1000
3	2	S10K275	590	920	S10K460	360	1430
4	4	S20K275 Q14K275	1560	900	S20K460	1300	1530

1.4 Interference emission

Switching off inductive loads can lead to overvoltages that may become sources of line interference as well as of inductively and/or capacitively coupled interference. This kind of interference can be suppressed using varistors connected as a flywheel circuit.

1.5 EMC systems engineering

EPCOS is your competent partner when it comes to solving EMC problems.
Our performance range covers:

- systems for measuring and testing EMC,
- shielded rooms for EMP measures,
- anechoic chambers,
- EMC consultation services and planning.

For further details, please refer to the “Chokes and Inductors” data book.

1.6 Protection of automotive electrical systems

1.6.1 Requirements

Electronic equipment must work reliably in its electromagnetic environment without, in turn, unduly influencing this environment. This requirement, known as electromagnetic compatibility (EMC), is especially important in automotive electrical systems, where energy of mJ levels is sufficient to disturb or destroy devices that are essential for safety. EPCOS has devised a wide range of special models matched to the particular demands encountered in automotive power supplies:

- extra high energy absorption (load dump),
- effective limiting of transients,
- low leakage current,
- jump-start capability (no varistor damage at double the car battery voltage),
- insensitivity to reverse polarity,
- wide range of operating temperature,
- high resistance to cyclic temperature stress.

EPCOS automotive varistors (SIOV-…AUTO) suit all these demands. They are specified separately in the product tables.

1.6.2 Transients

Standard ISO 7637 (DIN 40 839) details the EMC in automotive electrical systems. The toughest test for transient suppression is pulse 5, simulating load dump. This critical fault occurs when a battery is accidentally disconnected from the generator while the engine is running, e.g. because of a broken cable. Under this condition peak voltages up to 200 V can occur, lasting for few hundred ms, yielding energy levels up to 100 J. This worst case, as well as the other pulse loads, can be mastered reliably using SIOV-AUTO varistors.

1.6.3 Fine protection

Electronic components are often far apart, so EMC cannot be implemented with a central suppressor module alone. Instead you have to provide extra fine protection directly on the individual modules. Here energy absorption of a few Joules to some tens of Joules is adequate, meaning that lower rated and thus smaller components can be chosen. Figure 9 illustrates an EMC concept with varistors.

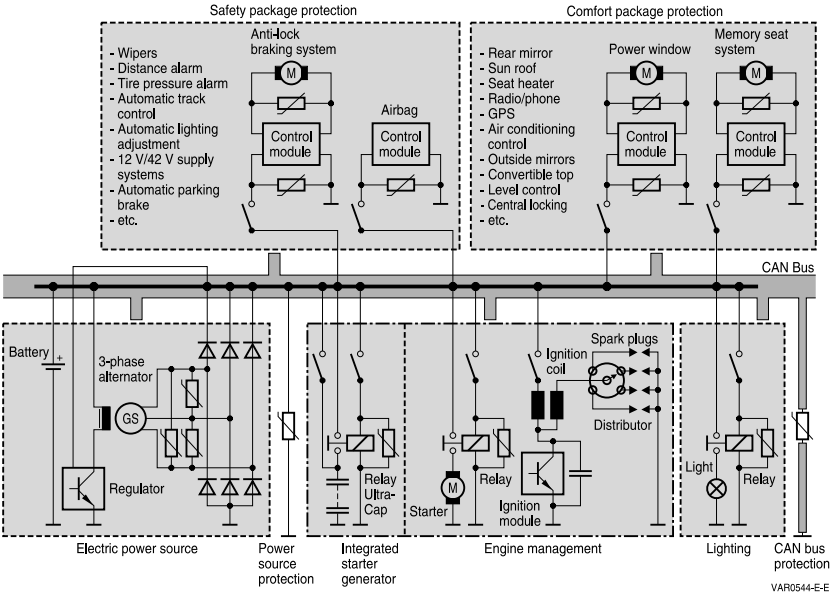
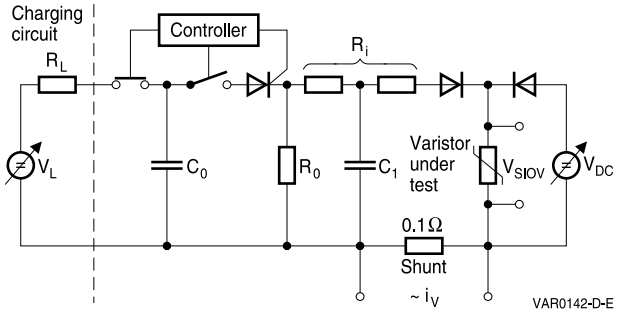


Figure 9 Automotive electrical system, complete EMC concept with varistors

1.6.4 Tests

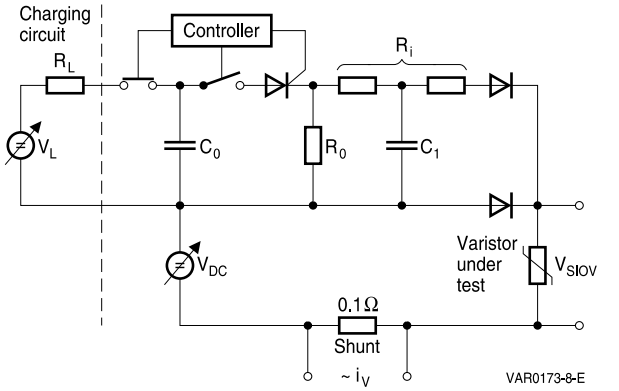
Maintenance of EMC requirements can be checked with conventional test generators. Figures 10 and 11 show block diagrams for load dump tests with operating voltage applied. The electrical performance associated with a load dump of 100 J is illustrated in figures 12 to 14.

Note:
Circuit 11 produces test pulse 5 according to ISO 7637 (DIN 40 839); the 10% time constant t_d can be set independently of battery voltage. Note that the maximum discharge current is not limited by the source V_{DC}.



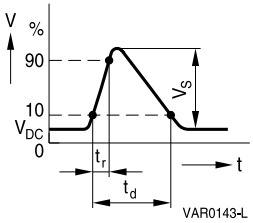
Typical values	
C_0	20 … 35 mF
R_0	4 … 10 Ω
C_1	0 … 10 µF
R_i	0.5 … 4 Ω
V_L	0 … 200 V
V_{DC}	12 … 28 V
t_d	100 … 800 ms
V_{SIOV}	Protection level of varistor
i_v	Current through varistor

Figure 10 Principle of load dump generator with battery connected in parallel



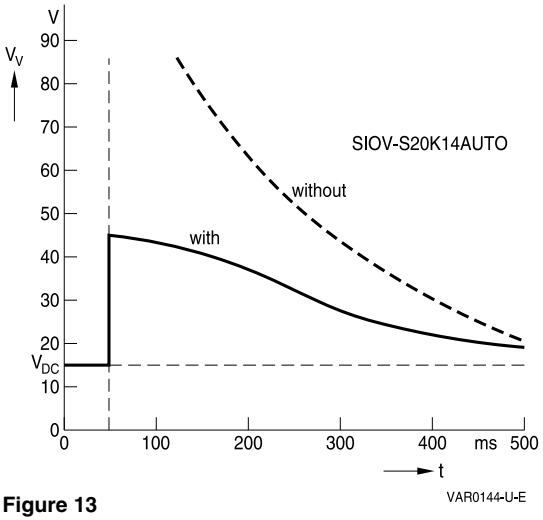
Typical values	
C_0	4.7 … 47 mF
R_0	4 … 5 Ω
C_1	47 … 470 µF
R_i	0.5 … 5 Ω
V_L	0 … 200 V
V_{DC}	12 … 28 V
t_d	40 … 500 ms
V_{SIOV}	Protection level of varistor
i_v	Current through varistor

Figure 11 Principle of load dump generator with battery connected in series



Test pulse 5
acc. to ISO 7637
(DIN 40 839)

Figure 12



Example:

C_0	= 37.6 mF
R_0	= 4.6 Ω
C_1	= 47 µF
V_S	= 146 V
V_{DC}	= 14 V
R_i	= 2 Ω
t_d	= 400 ms
t_r	= 0.1 ms

Figure 13

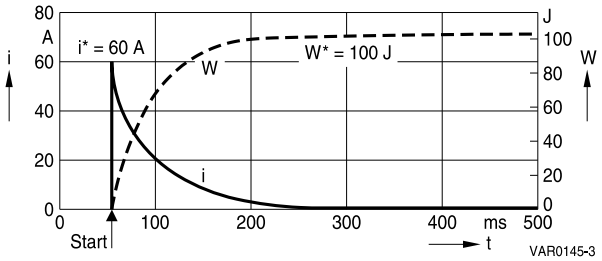


Figure 14

Voltage (figure 13), current and energy absorption (figure 14) on SIOV-S20K14AUTO with test pulse 5 (figure 14), load dump generator as in figure 11

1.6.5 Load dump simulation using PSpice software, e.g. PSpice simulation of the load dump energy

The time region of the varistor current derating graphs is only shown for up to 10 ms, whereas the load dump duration can be as long as 400 ms.

To cover also the load dump condition, the automotive product tables show supplementary maximum energy values for load dump absorption (10 ×).

In accordance with ISO 7637, the load dump pulse 5 is specified by the parameters

- Charge voltage (test level) V_s
- Internal resistance R_i
- Rise time t_r
- Duration t_d

(see figure 12).

The easiest way is to perform a software simulation (e.g. using PSpice) to determine the amount of energy dissipation by the varistor, which portion of the energy of this pulse the varistor absorbs. As stated in equation 10, the value calculated by this method must be lower than the value specified in the product tables.

ISO 7637 requires that at least one load dump absorption must be tolerated.

In other specifications repeated load dumps up to ten times are permissible. In coincidence with such regulations the automotive industry specifies load dump values for ten repetitions for their applications.

EPCOS offers to perform load dump simulations according to customers' specifications upon special request.

For such cases, we require information concerning:

V_s, R_i, t_r, t_d and the number of repetitions desired.

1.6.6 42 V vehicle power supply

For the 42 V vehicle on board power supply network, which will be of importance in the near future, EPCOS is offering the varistor type series SIOV-S ... V42AUTO. For details, please refer to the automotive product tables.

Remark: PSpice is a registered trademark of MicroSim Corporation.
For this software we offer varistor simulation models under www.epcos.com/tools_varistors.

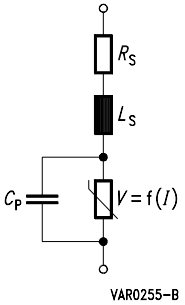
1.7 EPCOS PSpice simulation model

1.7.1 Varistor model

The development of a SIOV model for the “PSpice Design Center” circuit simulation program allows varistors to be integrated into the computer-assisted development of modern electronic circuitry.

In the PSpice modeling concept, the varistor is represented by its V/I characteristic curve, a parallel capacitance and a series inductance.

The structure of this equivalent circuit is shown in figure 15.



V = f (I)	V/I characteristic
C_p	Varistor capacitance
L_s	Series inductance
R_S = 100 μΩ	Series resistance

Figure 15 Varistor model, basic structure

In the model the V/I characteristic curve is implemented by a controlled voltage source V = f (I). An additional series resistance R_s = 100 μΩ has been inserted to prevent the impermissible state that would occur if ideal sources were to be connected in parallel or the varistor model were to be connected directly to a source.

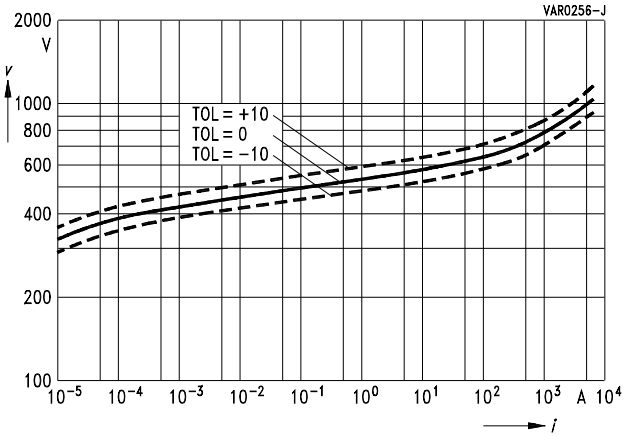
The following approximation is used for the mathematical description:

$$\log V = b1 + b2 \cdot \log (I) + b3 \cdot e^{-\log (I)} + b4 \cdot e^{\log (I)} \qquad I > 0 \qquad \text{(equ. 21)}$$

This means that the characteristic curve for any specific varistor can be described by the parameters b1 … b4. Figure 16 shows the typical V/I characteristic curve for the varistor SIOV-S20K275 and the corresponding parameters b1 … b4.

The tolerance bandwidth of the V/I characteristic curve can be shifted (cf. figures 14 and 15 in chapter “General technical information”) to include cases of

- upper tolerance bandwidth limit:
  highest possible protection level for a given surge current, and
- lower tolerance bandwidth limit:
  highest possible (leakage) current for a given voltage.



b1 = 2.7233755
b2 = 0.0258453
b3 = 0.0005746
b4 = 0.0046033

Figure 16 V/I characteristic curve of SIOV-S20K275 with tolerance band

In the model the capacitance values stated in the product tables are used. The dependence of the capacitance on the applied voltage and frequency is extremely low and can be neglected here.

It is not permissible to neglect the inductance of the varistor in applications with steep pulse leading edges. For this reason it is represented by a series inductance and essentially is determined by the lead inductance. As opposed to this, the internal inductance of the metal oxide varistor may be neglected. The inductance values in the model library are chosen for typical applications, e.g. approx. 13 nH for the S20K275. If longer leads are used, insertion of additional inductances must be considered if necessary. In the case of disk varistors the inductance of the leads is approx. 1 nH/mm.

The PSpice simulation models can be downloaded from the Internet (www.epcos.com/tools_varistors).

Limits of the varistor model

For mathematical reasons the V/I characteristic curves are extended in both directions beyond the current range (10 μA up to I_{max}) specified in this data book, and cannot be limited by the program procedure. The validity of the model breaks down if the specified current range is exceeded. For this reason it is imperative that the user consider these limits when specifying the task; the upper limit depends on the type of varistor. Values of < 10 μA may lead to incorrect results but do not endanger the component. In varistor applications it is only necessary to know the exact values for the leakage current in the < 10 μA range in exceptional cases. As opposed to this, values exceeding the type-specific surge current I_{max} may lead not only to incorrect results in actual practice but also to destruction of the component. Apart from this, the varistor model does not check adherence to other limit values such as maximum continuous power dissipation or surge current deratings. In addition to carrying out simulation procedures, adherence to such limits must always be ensured, observing the relevant spec given in the data book.

In critical applications the simulation result should be verified by a test circuit.

The model does not take into account the low temperature coefficient of the varistors (equ. 7).

1.7.2 Example for selection with PSpice

In this example the aim is to test whether selecting a standard varistor SIOV-S10K95 would meet the test conditions specified by the Germany's Central Telecommunications Engineering Bureau (FTZ):

Figure shows the test circuit with a 2 kV charge voltage, figure 17 shows the corresponding model used in PSpice.

To achieve an open-circuit voltage of 2 kV, the charging capacitor must be charged to 2.05 kV. To prevent an undefined floating of R_{m2}, an additional resistor R_1 = 10 MΩ is inserted at the output end.

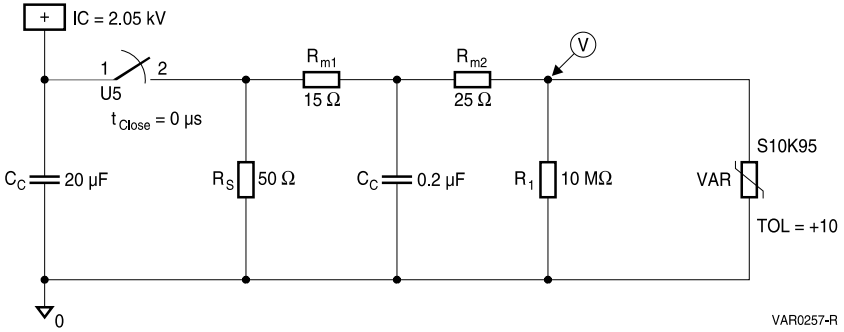


Figure 17 Simulation of the test pulse 10/700 µs applied to the device under test S10K95

For the varistor the upper characteristic curve tolerance (TOL = +10) limit is used to simulate the worst case, i.e. highest possible protection level. It is not considered necessary to model the device to be protected in this diagram since, in relation to the varistor, this is generally of higher resistance for pulse loads.

Figure 18 shows the curve of the open-circuit voltage (varistor disconnected) and the maximum protection level (with varistor).

Surge current

Figure 19 shows the voltage and current curves with the ∫i*d t included in the drawing.
A maximum current of 44 A can be deduced from the curves.

Then, according to equation 14:

$$t^*_r = \frac{\int i^* dt}{\hat{i}^*} = \frac{17\ mAs}{44\ A} \approx 386\ \mu s$$

According to figure , the resulting maximum surge current for 10 loads is

$I_{max} = 48\ A > \hat{i}^* = 44\ A.$

The selection criterion of equ. 9 is fulfilled.

Energy absorption

PSpice displays energy absorption directly as $W^* = \int v^* i^* d\,t = 4.2$ J.
The resulting permissible time interval between two pulses according to equation 20 is:

$$T_{min} = \frac{W^*}{P_{max}} = \frac{4.2\ J}{0.4\ W} = 10.5\ s$$

This means that the requirement of a minimum time interval between pulses of 60 s or more is fulfilled.

Highest possible protection level

Figure 18 shows the highest possible protection level to be 260 V. Thus it is possible to reduce the “overvoltage” of 2 kV to 13% of its value.

Note:
The specification stated above can also be met using the specially developed Telecom varistors (cf. section 1.8.2).

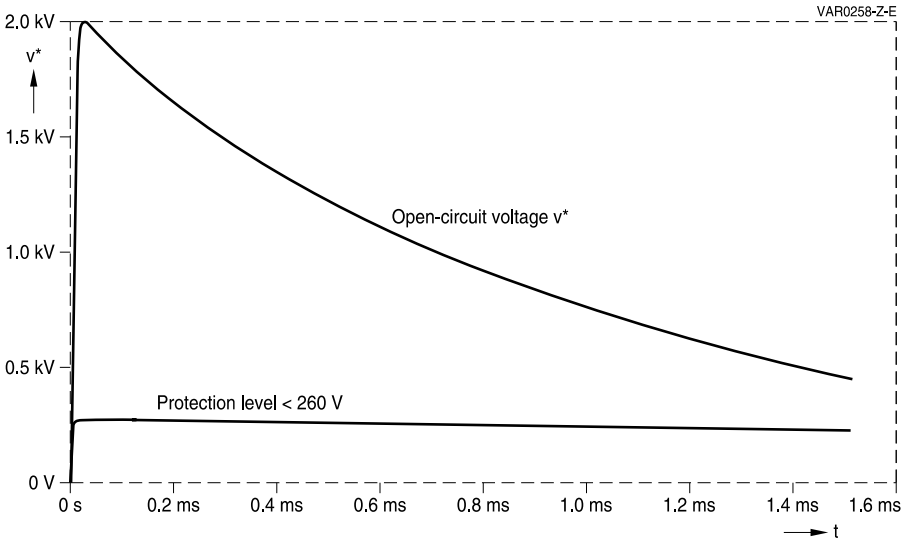


Figure 18 Open-circuit voltage (varistor disconnected) and maximum protection level (with varistor) achieved by the SIOV-S10K95 varistor

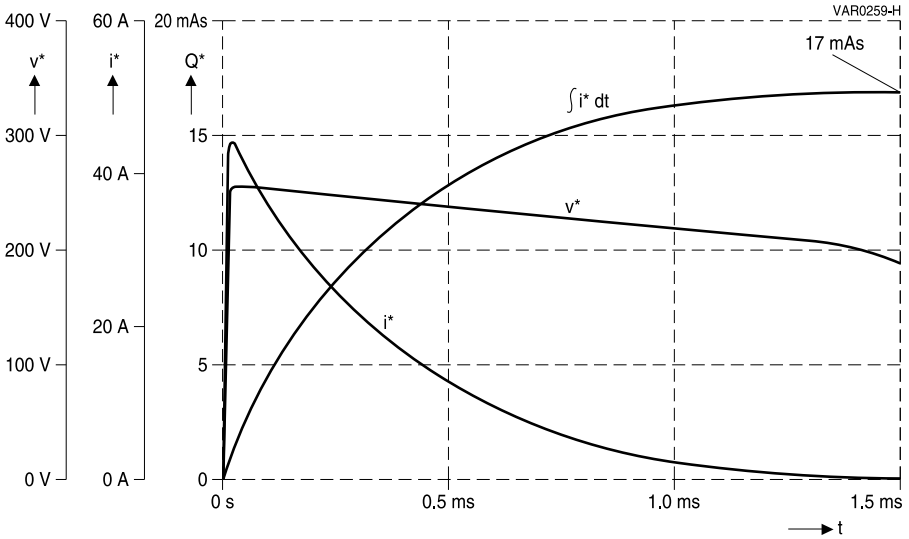


Figure 19 PSpice simulation: voltage, current and ∫i*d t curves for the S10K95

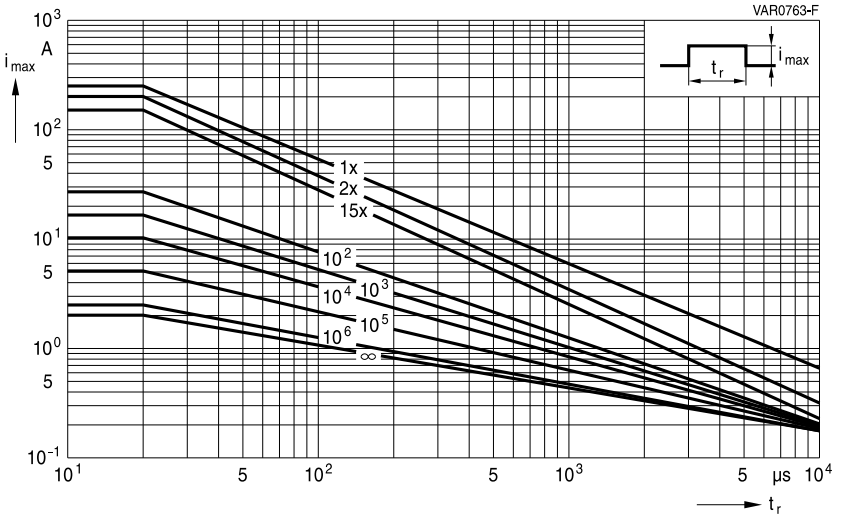


Figure 20 A maximum surge current i_{max} = 48 A (fifteen times) can be deduced for t^*_r = 386 µs from the derating curves for S10K50 … 320

1.8 Combined circuits

1.8.1 Stepped protection

If transient problems cannot be resolved with a single component like a varistor, it is always possible to combine different components and utilize their respective advantages. As an example, figure 21 illustrates the principle of stepped protection of a telemetry line with a gas-filled surge arrester[1], a varistor and a CeraDiode or suppressor diode[2]:

The voltage of 10 kV is limited in three stages

- "coarse" surge arrester
- "standard" varistor
- "fine" CeraDiode, suppressor diode[5], zener diode[5] or filter[3]

to less than 50 V. The series inductors or resistors are necessary to decouple the voltage stages.

Note:
According to the specifications in the "Product Profile"[4] gas-filled surge arresters may not be used on low-impedance supply lines.

1.8.2 Protective modules

Application-specific circuits for stepped protection assembled as modules, some incorporating overload protection and remote signaling, are available on the market.

Figures 21 and 23 show some practical examples.

1) Product Profile "Switching Spark Gaps"
2) Not in the EPCOS product range.
3) Data book "EMC Filters"

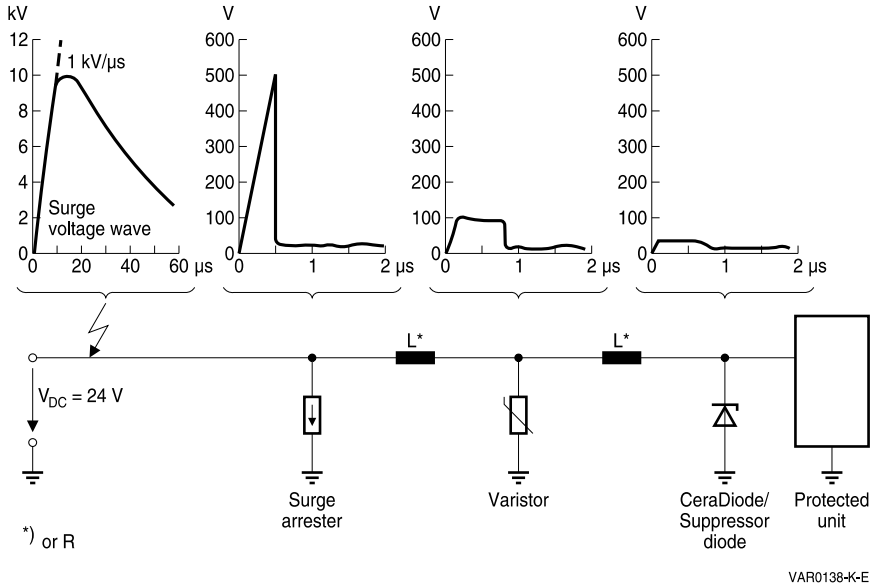


Figure 21 Principle of stepped protection with surge arrester, varistor and CeraDiode/suppressor diode

Examples of transient protective modules

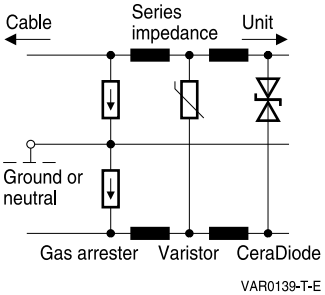


Figure 22 Circuit with coarse protection plus fine transverse voltage protection

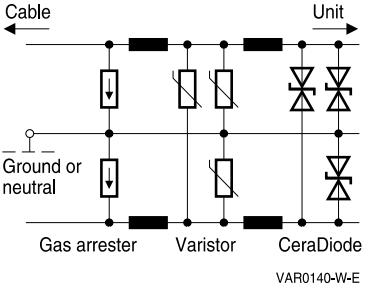


Figure 23 Circuit with coarse protection plus fine longitudinal voltage and transverse voltage protection